

A POSITION ENCODER PROCESSING UNIT

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Abstract

Typical motion controllers rely on a feedback position encoder to detect the actuator output and correct for external factors. Recent advancements in positioning systems increased the demand for the ability to process a variety of sensors and use the result to feedback the motion controller. In addition, data acquisition tools are becoming essential for metrology purposes to diagnose and analyse the behaviour of the system. A multi-sensor, multi-protocol unit with processing and data acquisition capabilities has been developed to address these requirements. Here we describe the main features of this unit, its internal architecture, and few examples of application.

INTRODUCTION

Modern high-accuracy positioning systems require a complex set of feedback information to correct the actuator position for external factors. The feedback information is obtained from several sensors that measure the position of the actuator, as well as any other relevant environmental physical quantities such as the temperature of the room.

The first difficulty with this approach is that typical motion controllers handle no more than one or two feedback sensors, usually a position encoder. That means that in multi-sensors cases, their information must be first processed and then synthesized as a single encoder for the motion controller. In other words, a mathematical function should be applied to the incoming data and the result be sent to the controller using an appropriated encoder protocol. This function will depend on the specificities of the system and therefore should be derived for each application.

Secondly, the encoders may use different protocols to transmit the measurement information. This requires appropriated readout devices to deal with each one of them. Popular encoders use quadrature signalling or SSI, BiSS-C, EnDat, and HSSL protocols. Moreover, not only can a system use encoders with different protocols but also similar encoders with distinct characteristics, for instance, two BiSS-C encoders with different data lengths.

The third and last aspect is the need of data acquisition capabilities for diagnostics and metrology purposes. The increasing complexity of high-accuracy systems demand sophisticated metrological tools to analyse their behaviour and performance. These tools should be able to retrieve the information from the relevant sensors, store it in a fast access buffer, and transfer it to the host computer for subsequent analysis.

Pre-engineered [1] and turnkey [2] solutions exist to deal with multi-protocol encoders processing. However, their specific architecture and considerable cost constitute an obstacle for generic applications at the ESRF. Thus, to address the features described above, a new electronic unit, PEPU, has been designed to handle up to six encoders with different protocols, process the received data according to a user-defined function, and emulate feedback information to the motion controller. In addition, PEPU has the necessary data acquisition capabilities for the needs of metrology of complex systems. The design has been carried out having in mind the specificities of the ESRF applications and the integration of the unit in the existing control environment.

The next section describes the functional aspects of PEPU and gives details about its internal architecture. Then, a section discusses the implementation aspects of the unit. The following section presents some examples of applications and, finally, the last section presents the conclusions and the future improvements.

FUNCTIONAL DESCRIPTION

The Fig. 1 depicts the PEPU functional block diagram.

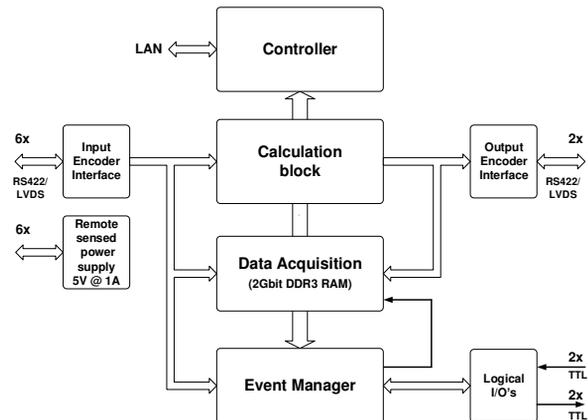


Figure 1: PEPU functional block diagram.

The controller allows the connection of PEPU to a host computer through the network (Ethernet) for remote control and data retrieval purposes. The controller treats, for instance, the configuration aspects by executing the commands received from the host.

On its side, the calculation block is in charge of performing operations on the incoming data according to a user-defined mathematical function. The outcome result can be transmitted through an output channel or pushed into the data acquisition buffer.

PEPU has six input channels that can handle both RS422 and LVDS signalling encoders. In addition, these

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six channels can also provide the encoders with a remote sensed power supply. The input channels can be individually configured to deal with incremental encoders as well as absolute encoder protocols such as SSI, BiSS-C, EnDat, and HSSL.

The unit has also two output channels to transmit data by means of an encoder protocol using either RS422 or LVDS electrical standards. These channels can generate quadrature signals and support the SSI, BiSS-C, and EnDat protocols. The information to be transmitted by these channels can be the outcome result of the processor of the input channels or the data provided by the host computer.

The data acquisition block deals with the collection and organization of data to be stored in its buffer. It contains a 2 Gbit memory that is filled up with the values of the channels or processing results selected by the user. The acquisition is synchronized with internal or external stimuli such as an order from the host, external trigger signals, internal timer, etc.

The event manager handles these synchronization and triggering aspects. Moreover, it controls two pairs of input and output signals used to synchronize with external devices. These signals are compatible with TTL levels.

IMPLEMENTATION

The Fig. 2 illustrates the implementation of the functionalities described in the previous section.

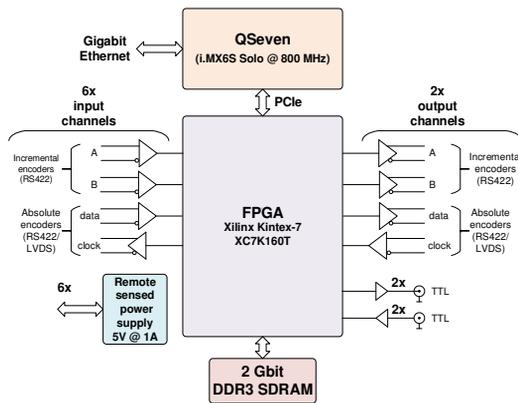


Figure 2: PEPU implementation block diagram.

The core of the PEPU hardware consists of a QSeven [3] single-board computer that runs a tailored Linux kernel in an NXP i.MX6S single-core 800 MHz ARM CPU along with a Xilinx Kintex-7 XC7K160T FPGA that is in charge of the low-level operations. These components communicate with each other through a PCIe link.

The QSeven module ensures the controller functions described in the previous section. It communicates with the host by means of bidirectional byte streams in which commands and responses are transferred as lines of printable ASCII characters through the network. In contrast, the transfer of larger volume of data is done in binary blocks for performance reasons.

The FPGA implements a PCIe endpoint that communicates with the internal HDL cores by means of the ESRF-developed E-bone [4]. It also implements the functions of the encoder interfacing, the calculation block, the data acquisition system, and the event management. The encoder interfacing is a highly configurable firmware module that handles the encoder protocols mentioned above. The code is written in such a way that each channel can be configured independently. The calculation block can execute up to eight functions simultaneously. Their values may not necessarily be associated to an output, but they can contain intermediate information for analysis purposes. At present, this block is limited to the execution of linear combinations of the input channels, but more complex functions can be introduced by means of a software plug-in. Presently, the plug-in is a small C-code that is executed by the controller. The current implementation refreshes the result of a linear combination in less than 1 μ s. On the other hand, even though the actual execution time of the plug-in is rather short, the controller can only guarantee a new value every 1 ms due to its non-real-time nature. The data acquisition system captures the values of pre-selected channels and manages their transfer to the embedded 2 Gbit DDR3 SDRAM and the subsequent transfer to the host. The event manager is responsible for the synchronization of the internal elements of PEPU and external devices.

The input and output channels consist of four pairs of differential signals to cover the needs for incremental and absolute encoders. All pairs are electrically compatible with the RS422 standard and two of them can be switched to LVDS. The RS422 electrical signalling rate can be as high as 50 MHz but this value should be derated according to the cable length. Similarly, the theoretical LVDS signalling can reach 400 MHz but the actual figures are more modest due to physical constraints such as the length of the cable. The direction of the differential drivers and receivers can be toggled to comply with the different protocols. For instance, SSI encoders require a clock input in order to output their data, whereas HSSL devices output both clock and data to the readout system.

The input channels can provide power to the encoders. PEPU implements 4-wire power supplies with remote sensing of the actual voltage over the encoder. The output channels do not provide power to the external devices.

Incidentally, the current implementation allows configuring two of the input channels as output to increase the flexibility of the unit.

Fast circuits able to produce pulses as short as 5 ns over 50-Ohm coaxial cables drive the two digital TTL outputs. The voltage levels at the receiver end are compatible with the TTL logic whether the cable terminates at high impedance or with a 50-Ohm load.

The two digital TTL inputs have the possibility of terminating or not with a 50-Ohm load by means of a front panel button or by software configuration. These inputs can detect pulses as short as 5 ns likewise the outputs.

PEPU is available in a standard 1U height 19-inch rack-mountable enclosure as illustrated in Fig. 3. The front

