

# PILOT APPLICATION OF NEW CONTROL SYSTEM AT SPring-8 RF TEST STAND

N. Hosoda<sup>1</sup>, T. Fukui, A. Gimenez, M. Ishii<sup>1</sup>, T. Ohshima<sup>1</sup>, M. Yamaga<sup>1</sup>,  
RIKEN, SPring-8 Center, Hyogo, 679-5148, Japan  
<sup>1</sup>JASRI, Hyogo, 679-5198, Japan

## Abstract

The SPring-8 upgrade project is in progress. The SACLALinac will be used as the injector of the SPring-8 storage ring. The MADOCA control framework was created 20 years ago and has contributed to the stable operation of both SPring-8 and SACLALinac. However, we must integrate separated control systems of two machines for the upgrade. In addition, some new ICT standard protocols designed recently have the potential to simplify the implementation of the framework. With these background, we have developed a new messaging system MS-MQTT and a new DAQ system MDAQ, based on the concepts of simple, easy management and unified operation covering SPring-8 and SACLALinac. For the equipment control hardware, we have adopted the modern architecture of MTCA.4 and EtherCAT. We are developing a universal driver for MTCA.4 modules. A pilot application of the new control system including the new hardware was performed at the RF test stand. The result of high power RF operation showed that the high stability required for the RF amplitude and phase in the cavity was achieved using the new system. We confirmed that the new framework can control SPring-8-II.

## INTRODUCTION

SPring-8 is a third-generation X-ray synchrotron radiation source that has been operating since 1997. It consists of a 1 GeV linac, an 8 GeV booster synchrotron and an 8 GeV storage ring. SACLALinac is an X-ray free-electron laser source that has been operating next to SPring-8 since 2012. A low emittance electron beam is generated from an 8 GeV linac of SACLALinac. SPring-8 and SACLALinac are currently operated independently.

In 2014, a conceptual design of upgrading SPring-8 to an ultralow-emittance ( $\sim 100$  pmrad) ring, SPring-8-II, was decided [1, 2]. One of the important concepts of the upgrade is to use the linac of SACLALinac as the injector of the storage ring of SPring-8-II. This means that we must operate two machines cooperatively. Another important concept is to minimize the blackout period during users are forced to stop their experiments. We should carry out the upgrade plan carefully with as many preliminary studies of the new system as possible.

The MADOCA control framework [3] was created 20 years ago to control the SPring-8 storage ring which works as a DC machine. When we constructed SACLALinac, it was natural for us to adopt MADOCA for the SACLALinac control system [4]. However, we had to add a synchronous data acquisition (DAQ) system that was not in the original framework [5]. Because SACLALinac is a pulsed machine with a repetition rate of 60 Hz, equipment data arising from the

pulsed electron beam should be collected synchronously. To keep the operation of two machines independent, we prepared different databases for them. And we also separated control networks of two machines by a firewall.

For SPring-8-II, we must integrate both control systems to enable seamless operation of two machines [6]. We redesigned some points to be improved in current control framework to facilitate the integration. The design concepts were simple, easy management, unified operation and positive use of new ICT standard systems/protocols introduced in the last decade.

For example, in the messaging, the message server used to communicate between hosts is run in each host. The server reads a list of signal names and corresponding host names from a file prepared in each host. Because the server uses queues without flow control, the mixing of reply messages could occur. We created new messaging system not to use any files and no mixing of reply messages using MQTT. In the DAQ system, a signal list to collect data from equipment is also prepared in each host. The collected data are gathered in a collector host then written to the database. The fixed-period DAQ system and the synchronized DAQ system added to SACLALinac later are operated independently in terms of the databases. We created a unified DAQ system using Cassandra and MariaDB

The situation is the same for the hardware. Although we still use VME, RS-232C and so forth, we decided to introduce the leading-edge hardware architectures of MTCA.4 and EtherCAT. For MTCA.4 we inherited the idea of a universal driver from DESY and modified it for our usage.

In this paper, we describe the pilot application of the new control system to prove the operation feasibility at the RF test stand of SPring-8.

## NEW CONTROL FRAMEWORK

### MS-MQTT

The MQTT is a publish-subscribe-based “lightweight” messaging protocol suited for IoT. MS-MQTT is a newly developed messaging scheme that uses MQTT to access equipment from an operator console. Its features are (a) only one MQTT broker (server) in the control network, (b) no server process in each client host, (c) a simple structure with easy management, (d) no mixing of reply messages owing to no queue or flow control, (e) increased speed using multiple threads and sequence control by distributed processing due to asynchronous processing of messages and (f) simultaneous message transmission to multiple hosts.

When a control process is launched, it subscribes topics that include all signal object names treated in the process

Content from this work may be used under the terms of the CC BY 3.0 licence (© 2017). Any distribution of this work must maintain attribution to the author(s), title of the work, publisher, and DOI.

to the MQTT broker and waits for messages. When an operator wants to access equipment, the GUI process in the operator console publishes a message including a signal object name to be accessed. Then the message is delivered to the target process via the MQTT broker. We designed MS-MQTT to return a reply from the initial subscriber to the initial publisher so that the equipment control is reliably carried out.

### MDAQ

To monitor equipment signals periodically, we developed an MDAQ process. The features of the MDAQ are (A) reading parameter settings, such as a signal list and an acquisition interval from a database, (B) direct writing collected data to the database without any intermediate host, (C) easily scaled up with increasing numbers of hosts, (D) simple to manage, (E) support ability for the synchronized DAQ which is used at SACLA, and (F) integrated with an online database using a Cassandra.

The MDAQ consists of an event watcher thread and a DAQ thread. The DAQ thread reads a list of signal object names to be collected from a parameter database. The event watcher thread periodically calls the DAQ thread, then it writes collected data to the online database directly. The online data is reduced to a 60 second period and permanently stored in an archive database. In addition to the fixed-period event watcher thread, we prepared an external trigger event watcher thread to deal with the synchronized DAQ.

### MTCA.4

After 20 years of successful operation of SPring-8, maintaining the old analogue modules of the LLRF system tends to be difficult. Meanwhile digital technologies such as FPGA and fast ADC/DAC have become popular. We decided to replace the old analogue LLRF system in SPring-8 with a modern MTCA.4-based one [7, 8].

### Universal Driver for MTCA.4

In terms of software development, it is ideal to use different digitizers without any modification of the source code for application processes.

The original idea of the universal driver for MTCA.4 was developed at DESY [9]. There are two driver layers. One is a hardware bus and OS specific driver. In our case, the hardware bus is PCI Express and the OS is Linux. The other is a hardware specific driver. Because we have had experiences in developing a nexus driver and leaf driver for Solaris OS on a VME system, we could incorporate this idea smoothly.

Figure 1 shows the system structure of the universal driver for MTCA.4 at SPring-8. The bus driver is a hardware bus/OS specific layer. It is common for child drivers. The child driver is a hardware-specific layer in the kernel. The driver shim is a hardware-specific layer used to transfer data from the user space to the kernel space. Devapi is a generic API layer and an object-oriented layer. We do not have to pay attention to hardware when we program applications.

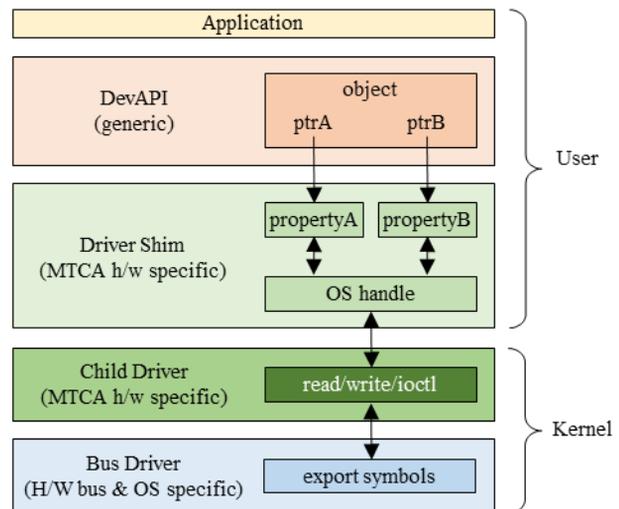


Figure 1: System structure of the universal driver for MTCA.4 at SPring-8.

### EtherCAT

We have adopted EtherCAT as the standard field bus of SPring-8-II [10]. It is used for slow control of the equipment. The EtherCAT modules are wired in a daisy chain topology with Ethernet cables. The reduced wiring is one of the advantages of EtherCAT.

## APPLICATION OF NEW CONTROL SYSTEM TO RF POWER CONTROL

Prior to replacing the system in SPring-8, we examined the performance of the new system at an RF test stand. A block diagram of the RF test stand is shown in Figure 2.

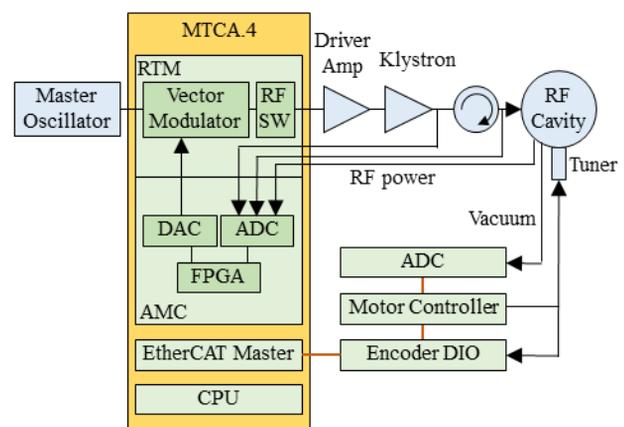


Figure 2: Block diagram of the RF test stand with MTCA.4 and EtherCAT.

The reference RF signal generated by the master oscillator is fed to the klystron through a vector modulator. The amplified RF signal by the klystron is fed to the RF cavity. The phase and amplitude of the cavity pickup signal is calculated from the ADC data. The FPGA firmware works to

keep the phase and amplitude to the set values by adjusting the control voltage fed to the vector modulator. An SIS8300L2 AMC digitizer and a DWC8VM1 RTM vector modulator manufactured by Struck innovative systems were used for the test. The digitizer was equipped with 10-channel, 125 MS/s, 16-bit ADCs, two 250 MS/s 16-bit DACs, and a Vertex 6 FPGA. Two feedback control functions, which originally consisted of analogue modules, were reproduced in the FPGA of the digitizer. We selected a Schroff MTCA.4 chassis, an MCH, and an RTM CPU module manufactured by NAT. An EtherCAT master modules, Advanet AdXMC1573 XMC was mounted on a Vatech AMC105 PMC/XMC carrier, and installed in the MTCA.4 chassis. The slaves were a Melec F3200/EC for the motor control of the cavity tuner, two CEC ECAT-S-DIOs for the tuner encoder readout, and a Sinfonia technology AI0816 to read the vacuum pressure of the cavity and some voltages of the klystron power supply.

Figure 3 shows a block diagram of the control system at the RF test stand.

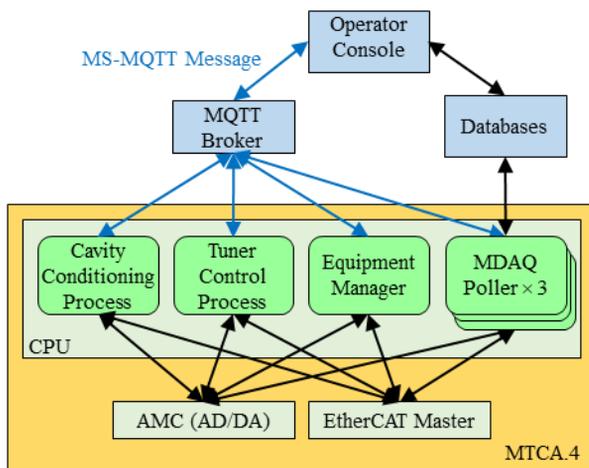


Figure 3: Block diagram of the control system at RF test stand.

The operating system of the processor CPU is Ubuntu 14.04 LTS with a low-latency kernel. We prepared four kinds of Linux processes. The equipment manager (EM) is the most basic process and is used to access all equipment control modules. The cavity conditioning process increases the klystron power by monitoring the cavity vacuum pressure to avoid breakdown at an input RF coupler. The tuner control process keeps the RF reflection power at a minimum by adjusting the cavity tuner position by observing the phase difference between the cavity input signal and the cavity pickup signal. The GUI process in the operator console exchange control messages with these processes in the MTCA.4 via MQTT broker. The specifications of the MQTT broker are an eMQTT 2.0.7 on a CentOS 6.5 (x86\_64) of a DELL PowerEdge R210 with 16 GB RAM. The MDAC is the fixed-period DAQ process. We prepared three MDAQ processes with a 1 s period for an AMC digitizer, a 5 s period for RTM power and temperature signals

and a 2 s period for EtherCAT signals. The parameter database is MariaDB 10.1.9 on CentOS 6.5 (x86\_64) of a Proliant DL120 Gen9 with 24 GB RAM. The online database is Cassandra 2.1.10 on a CentOS 6.7 (x86\_64) of a JSC Vintage 3U with 16 GB and 12 nodes. The archive database is on the same machine as the parameter database.

After the preparation of the new control system at the RF test stand, a high-power RF operation was carried out. Typical data collected by the MDAQ are shown in Figure 4. The graph shows that the speed required to increase the klystron output power was high when the cavity pressure was low, but the required speed became low when the pressure reached the upper limit as expected. The cavity conditioning process thus worked well.

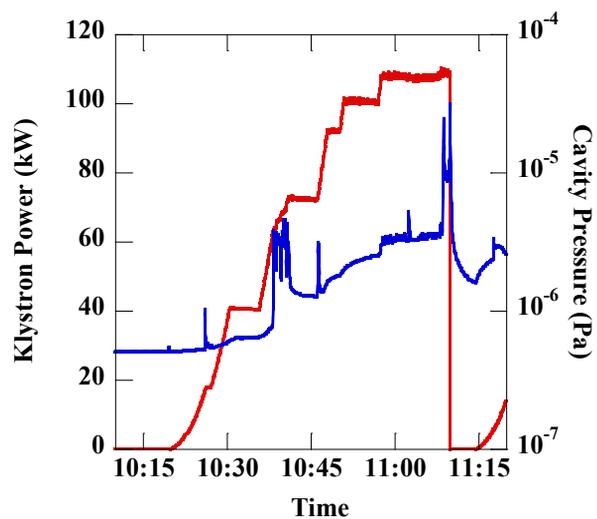


Figure 4: Typical data collected by the MDAQ.

Currently, we are developing a new MMEADC01B AMC digitizer equipped with 10-channels, 370 MS/s, 16-bit ADCs, two 500 MS/s, 16-bit DACs, and a Kintex 7 FPGA. It will be tested at the RF test stand and installed in LLRF of SPring-8-II.

## SUMMARY

Following the successful high-power RF operation at the RF test stand, we are confident that the new system has sufficient capability to control SPring-8-II. This summer, as the second application of the new system, it was successfully applied to the dedicated accelerator for the soft X-ray free-electron laser beam line of SACLA, which is a small accelerator at the SPring-8 site [11]. We will apply the system to the SPring-8 storage ring this winter and to SACLA next summer.

## REFERENCES

- [1] H. Tanaka et al., "SPring-8 upgrade project", Proc. of IPAC2016, Busan, Korea, May 2016, paper MOPW009, pp. 2867-2870.

Content from this work may be used under the terms of the CC BY 3.0 licence (© 2017). Any distribution of this work must maintain attribution to the author(s), title of the work, publisher, and DOI.

- [2] “SPring-8-II Conceptual Design Report”, RIKEN SPring-8 Center, 2014, <http://rsc.riken.jp/pdf/SPring-8-II.pdf>.
- [3] R. Tanaka et al., “Control System of the SPring-8 Storage Ring”, Proc. of ICALEPCS’95, Chicago, USA, October 1995, pp.201.
- [4] T. Fukui, et al., “Status of the X-ray FEL control system at SPring-8”, Proc. of ICALEPCS2007, Tennessee, USA, October 2007.
- [5] M. Yamaga et al., “Event-synchronized data acquisition system for SPring-8 XFEL”, Proc. of ICALEPCS2009, Kobe, Japan, October 2009, paper TUB003, pp 69-71.
- [6] T. Fukui et al., “Status of the control system for the SACLA/SPring-8 Accelerator complex”, Proc. of ICALEPCS2017, Barcelona, Spain, October 2017, paper FRAPL03, this conference.
- [7] H. Ego et al., “RF system of the SPring-8 upgrade project”, Proc. of IPAC2016, Busan, Korea, May 2016, paper MOPW009, pp. 414-416.
- [8] T. Ohshima et al., “Development of a new LLRF system based on microTCA.4 for the SPring-8 storage ring”, Proc. of IPAC2017, Copenhagen, Denmark, May 2017, paper THPAB117, pp. 3996-3999.
- [9] L. Petrosyan et al., “Linux Universal PCI Express Device Drivers for MTCA”, Proc. of ICALEPCS2017, Barcelona, Spain, October 2017, paper TUPHA151, this conference.
- [10] M. Ishii et al., “Next generation control system using the EtherCAT technology”, Proc. of ICALEPCS2017, Barcelona, Spain, October 2017, paper TUPHA148, this conference.
- [11] N. Hosoda et al., “Control system for a dedicated accelerator for SACLA wide-band beam line”, Proc. of ICALEPCS2015, Melbourne, Australia, October 2015, paper MOM305, pp. 74-78.